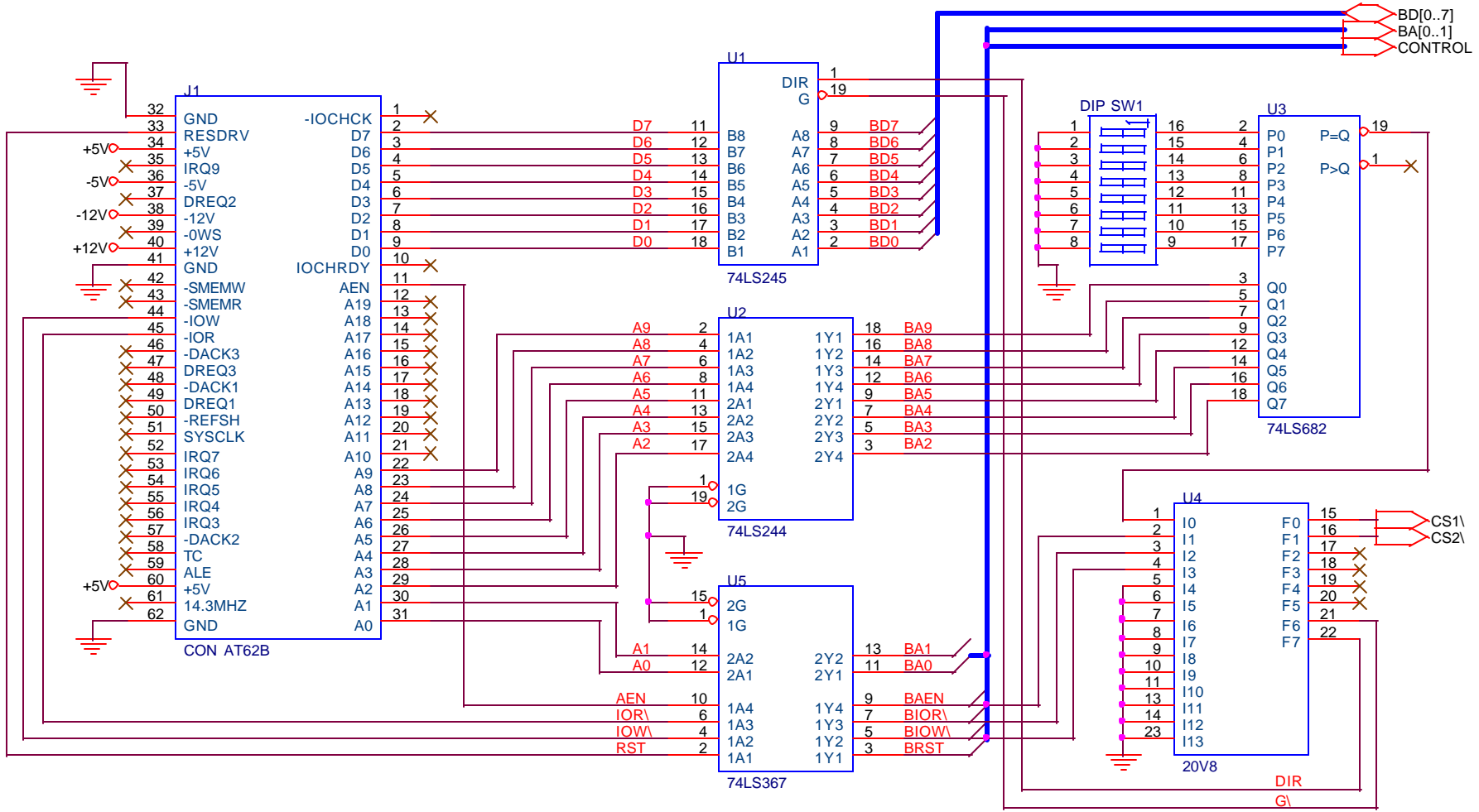


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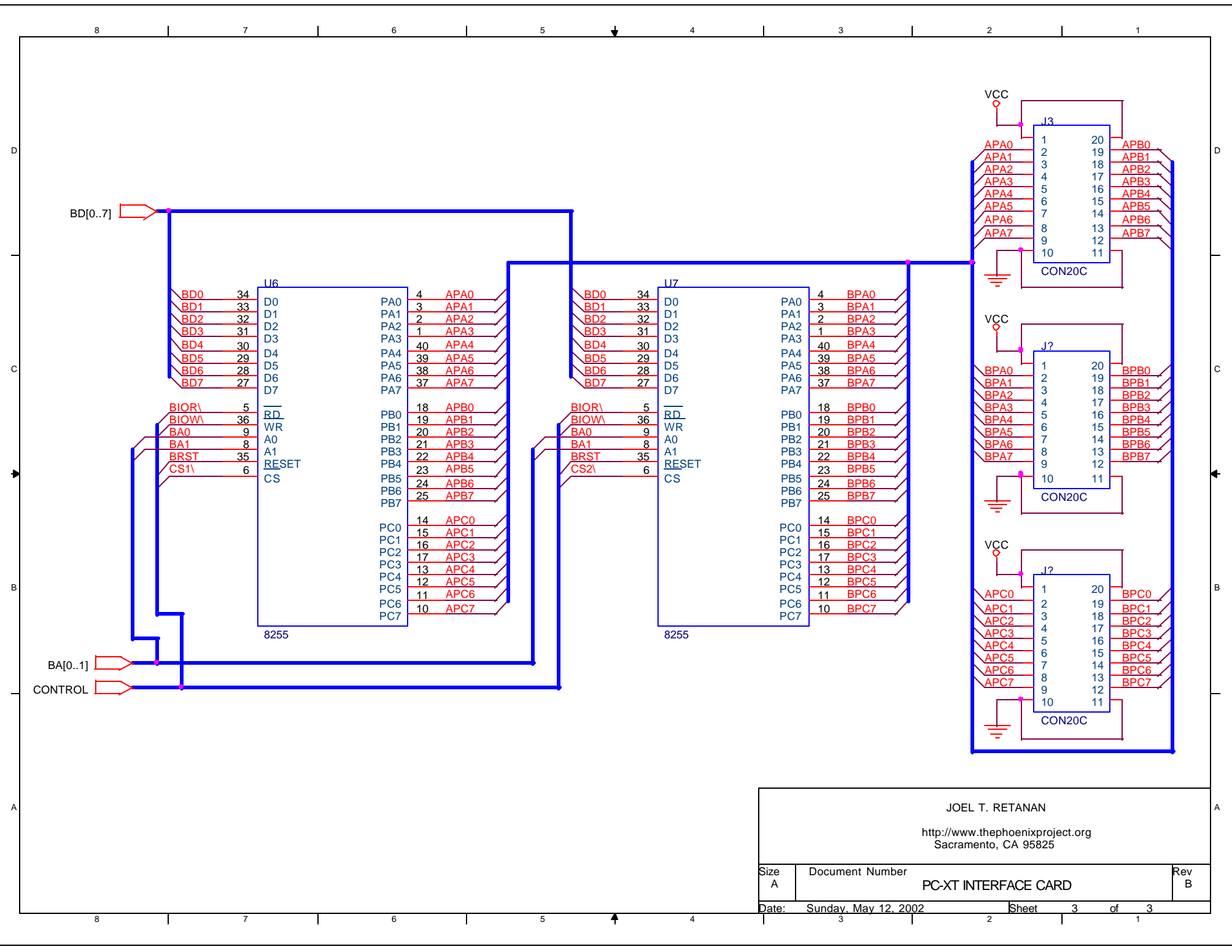
<http://www.thephoenixproject.org>
 Sacramento, CA 95825

Size A	Document Number PC-XT INTERFACE CARD	Rev B
Date: Sunday, May 12, 2002	Sheet 1 of 3	



JOEL T. RETANAN
<http://www.thephoenixproject.org>
 Sacramento, CA 95825

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JOEL T. RETANAN

<http://www.thephoenixproject.org>
 Sacramento, CA 95825

Revised: Sunday, May 12, 2002

PC-XT INTERFACE CARD

Revision: B

JOEL T. RETANAN

<http://www.thephoenixproject.org>

Sacramento, CA 95825

Bill Of Materials

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Item	Quantity	Reference	Part
1	1	DIP SW1	SW DIP-8
2	2	J?,J3	CON20C
3	1	J1	CON AT62B
4	1	U1	74LS245
5	1	U2	74LS244
6	1	U3	74LS682
7	1	U4	20V8
8	1	U5	74LS367
9	2	U6,U7	8255

```

module PCINTERF          flag '-r3';

title 'PC-XT Interface Card Decoder
Joel T. Retanan          March 27, 1994';

"This design may be expanded for future change or improvement.

        U4  device 'P20V8R';

"Power:
        VCC, GND                pin 24,12;

"Inputs:
        AEN, IORn, IOWn         pin 2,3,4;
        P_EQ_Qn                 pin 1;

"outputs:
        CS1n                    pin 15;
        ENAn, DIR               pin 21,22;

equations
        !CS1n = (!IORn # !IOWn) & !AEN & !P_EQ_Qn;
        !ENAn  = (!IORn # !IOWn) & !AEN & !P_EQ_Qn;
        DIR    = !IORn & IOWn;

test_vectors
        ([ P_EQ_Qn, AEN, IORn, IOWn ] -> [ CS1n, ENAn, DIR ])
        [ 0, 0, 0, 0 ] -> [ 0, 0, 0 ];
        [ 0, 0, 0, 1 ] -> [ 0, 0, 1 ];

        [ 0, 0, 1, 0 ] -> [ 0, 0, 0 ];
        [ 0, 0, 1, 1 ] -> [ 1, 1, 0 ];
        [ 0, 1, 0, 0 ] -> [ 1, 1, 0 ];
        [ 0, 1, 0, 1 ] -> [ 1, 1, 1 ];

        [ 0, 1, 1, 0 ] -> [ 1, 1, 0 ];
        [ 0, 1, 1, 1 ] -> [ 1, 1, 0 ];
        [ 1, 0, 0, 0 ] -> [ 1, 1, 0 ];
        [ 1, 0, 0, 1 ] -> [ 1, 1, 1 ];

        [ 1, 0, 1, 0 ] -> [ 1, 1, 0 ];
        [ 1, 0, 1, 1 ] -> [ 1, 1, 0 ];
        [ 1, 1, 0, 0 ] -> [ 1, 1, 0 ];
        [ 1, 1, 0, 1 ] -> [ 1, 1, 1 ];

        [ 1, 1, 1, 0 ] -> [ 1, 1, 0 ];
        [ 1, 1, 1, 1 ] -> [ 1, 1, 0 ];

end PCINTERF

```